	Document ID	Issue Date	Pages	Title	Inventor
1	US 20060061399 A1	20060323	25	Programmable high-resolution timing jitter injectors	Xu; Jianping et al.
2	US 20050264336 A1	20051201	14	Differential type delay cells and methods of operating the same	Kang, Dae-Woon
3	US 20030030498 A1	20030213	16	Two stage VCO circuit with low voltage and power requirements	Eatock, Frederick L.
4	US 20020145460 A1	20021010	7	High speed, low-power CMOS circuit with constant output swing and variable time delay for a voltage controlled oscillator	Lin, Xijian et al.
5	US 20010009392 A1	20010726	18	Voltage-controlled oscillator	Soda, Masaaki
6	US 7205813 B2	20070417	14	Differential type delay cells and methods of operating the same	Kang; Dae-Woon
7	US 7176737 B2	20070213	17	Phase-locked loop and delay-locked loop including differential delay cells having differential control inputs	Baker; Michael P. et al.
8	US 7106142 B2	20060912	9	Ring-type voltage oscillator with improved duty cycle	Lin; Yu-Hong
9	US 6894552 B2	20050517	9	Low-jitter delay cell	Iorga; Cosmin et al.
10	US 6870415 B2	20050322	18	Delay generator with controlled delay circuit	Zhang; Bo et al.
11	US RE38499 E	20040420	14	Two-stage amplifier for active pixel sensor cell array for reducing fixed pattern noise in the array output	Merrill; Richard B. et al.
12	US 6724230 B2	20040420	13	Semiconductor integrated circuit	Hirabayashi; Osamu
13	US RE38482 E	20040330	29	Delay stage circuitry for a ring oscillator	Leung; Wingyu et al.
14	US 6642761 B1	20031104	9	Interface circuit of various clock period between a fast slope signal and a very slow slope, voltage controlled delay cell	Tien; Li-Chin
15	US 6593820 B2	20030715	15	High frequency voltage controlled oscillator	Eatock; Frederick L.

	Document ID	Issue Date	Pages	Title	Inventor
16	US 6570427 B2	20030527	15	Variable transconductance amplifier	Prentice; John S.
17	US 6525586 B1	20030225	12	Programmable delay element using differential technique	Ahmed; Abdullah et al.
18	US 6512420 B1	20030128	10	Variable frequency oscillator utilizing selectively combined dual delay paths	Eker; Mehmet M et al.
19	US 6501317 B2	20021231	6	High speed, low-power CMOS circuit with constant output swing and variable time delay for a voltage controlled oscillator	Lin; Xijian et al.
20	US 6377095 B1	20020423	20	Digital-edge-rate control LVDS driver	Kuo; James R.
21	US 6351191 B1	20020226	10	Differential delay cell with common delay control and power supply	Nair; Rajendran et al.
22	US 6304150 B1	20011016	13	Double-clamped delay stage and voltage controlled oscillator	Shenoy; Ravindra
23	US 6288588 B1	20010911	7	Programmable delay circuit	Frisch; Arnold M.
24	US 6255881 B1	20010703	6	High tunability CMOS delay element	Balistreri; Emanuele et al.
25	US 6175260 B1	20010116	14	Time delay apparatus using transfer conductance	Cho; Gea-ok
26	US 6107854 A	20000822	14	Variable speed path circuit and method	Wong; Wilson et al.
27	US 6060939 A	20000509	17	Digitally controlled differential delay line circuit and method of controlling same	Woeste; Dana Marie et al.
28	US 6052003 A	20000418	15	CMOS delay circuit	Molin; Stuart B. et al.
29	US 5994939 A	19991130	12	Variable delay cell with a self-biasing load	Johnson; Luke A. et al.
30	US 5982214 A	19991109	8	Variable delay circuit	Kim; Chang-Sun
31	US 5945863 A	19990831	6	Analog delay circuit	Coy; Bruce H.
32	US 5936475 A	19990810	9	High-speed ring oscillator	Tchamov; Nikolay et al.
33	US 5799051 A	19980825	25	Delay stage circuitry for a ring oscillator	Leung; Wingyu et al.
34	US 5793239 A	19980811	10	Composite load circuit	Kovacs; Janos et al.

	Document ID	Issue Date	Pages	Title	Inventor
35	US 5783953 A	19980721	7	CMOS current controlled delay element using cascoded complementary differential amplifiers with replicated bias clamp	Bosnyak; Robert J. et al.
36	US 5777501 A	19980707	8	Digital delay line for a reduced jitter digital delay lock loop	AbouSeido; Maamoun
37	US 5721875 A	19980224	14	I/O transceiver having a pulsed latch receiver circuit	Fletcher; Tom D. et al.
38	US 5721505 A	19980224	10	Delay circuit manufacturable by semiconductor elements	Tsuchiya; Chikara
39	US 5717362 A	19980210	37	Array oscillator circuit	Maneatis; John George et al.
40	US 5625312 A	19970429	8	Control circuit for semiconductor device	Kawakami; Hiroyuki et al.
41	US 5596610 A	19970121	24	Delay stage circuitry for a ring oscillator	Leung; Wingyu et al.
42	US 5550503 A	19960827	13	Circuits and method for reducing voltage error when charging and discharging a capacitor through a transmission gate	Garrity; Doug et al.
43	US 5521558 A	19960528	5	Inverter stage having diode load and ring oscillator using same	Wilhelm; Wilhelm et al.
44	US 5521539 A	19960528	15	Delay line providing an adjustable delay	Molin; Stuart B.
45	US 5479045 A	19951226	19	Semiconductor circuit device capable of reducing influence of a parasitic capacitor	Narahara; Tetsuya et al.
46	US 5243240 A	19930907	20	Pulse signal generator having delay stages and feedback path to control delay time	Murakami; Daisuke et al.
47	US 5229664 A	19930720	9	Programmable differentiator delay	Brehmer; Kevin E.
48	US 5182480 A	19930126	6	Pulse delay circuit having two comparators	Goto; Kuniaki
49	US 5160863 A	19921103	15	Delay circuit using primarily a transistor's parasitic capacitance	Hui; Titkwan
50	US 5144174 A	19920901	9	Programmable delay circuit having a buffer stage connected in cascode between the outputs of a plurality of differential amplifiers and the output terminal	Murakami; Daisuke
51	US 5144173 A	19920901	15	Programmable delay line integrated circuit having programmable resistor circuit	Hui; Titkwan

	Document ID	Issue Date	Pages	Title	Inventor
52	US 5120985 A	19920609	28	Data reproducing circuit for correcting amplitude variation and peak shift	Kimura; Toshiki
53	US 5087842 A	19920211	7	Delay circuit having one of a plurality of delay lines which may be selected to provide an operation of a ring oscillator	Pulsipher; James A. et al.
54	US 5066877 A	19911119	19	Data delay circuit and clock extraction circuit using the same	Hamano; Hiroshi et al.
55	US 5015872 A	19910514	13	Method and circuit arrangement for generating a phase shifted clock pulse signal	Rein; Hans-Martin
56	US 4893036 A	19900109	8	Differential signal delay circuit	Hester; Richard E. et al.
57	US 4820944 A	19890411	12	Method and apparatus for dynamically controlling the timing of signals in automatic test systems	Herlein; Richard F. et al.
58	US 4797586 A	19890110	13	Controllable delay circuit	Traa; Einar O.
59	US 4794275 A	19881227	10	Multiple phase clock generator	Traa; Einar O.
60	US 4763029 A	19880809	8	Triggered voltage controlled oscillator using fast recovery gate	Caspell; George J.
61	US 4739277 A	19880419	17	Triggered, programmable skew signal generator	Hollister; Allen L. et al.
62	US 4647791 A	19870303	6	Generator for producing multiple signals which are synchronous with each other	Pellegrini; Franco
63	US 4641048 A	19870203	6	Digital integrated circuit propagation delay time controller	Pollock; Ira G.
64	US 4611136 A	19860909	10	Signal delay generating circuit	Fujie; Norikazu
65	US 4604536 A	19860805	5	Timing circuits	Clutterbuck; Richard C. D. et al.
66	US 4359689 A	19821116	12	Clock pulse driver	Guenthner; Russell W.
67	US 4338532 A	19820706	8	Integrated delay circuits	Houghton; Russell J.
68	US 4321482 A	19820323	7	Circuit system for the generation of a direct control voltage which is dependent on an alternating voltage	Schroder; Ernst et al.
69	US 4001698 A	19770104	9	Analog timer including controllable operate-recovery time constants	Allred; Ralph Rabun

	Document ID	Issue Date	Pages	Title	Inventor
70	US 3943385 A	19760309	7	Time switch circuit having a switch-back time delay	Achtstaetter; Gerhard
71	US 3889197 A	19750610	14	Timer apparatus utilizing operational amplifier integrating means	Duff; Thomas Guy
72	US 3836791 A	19740917	7	PRESETTABLE SINGLE-INPUT VOLTAGE-TIME INTEGRATOR	Galloway; Glen L.
73	US 3808466 A	19740430	7	CAPACITIVE-DISCHARGE TIMING CIRCUIT USING COMPARATOR TRANSISTOR BASE CURRENT TO DETERMINE DISCHARGE RATE	Campbell; Leonard Richard
74	US 3654494 A	19720404	7	CAPACITOR TYPE TIMING CIRCUIT UTILIZING ENERGIZED VOLTAGE COMPARATOR	Bartlett; Peter G. et al.
75	US 3602743 A	19710831	5	CIRCUIT FOR PRODUCING AN OUTPUT PULSE OF PREDETERMINED WIDTH AFTER A PREDETERMINED DELAY	De Shazo, Jr.; Earl L.
76	US 3581215 A	19710525	5	VARIABLE FREQUENCY DELAY LINE DIFFERENTIATOR	Meyer; Forrest C.
77	US 3575618 A	19710420	5	APPARATUS FOR PROVIDING AN ACCURATELY DELAYED OUTPUT PULSE OF ACCURATELY PREDETERMINED DURATION	Kawabata; Frederick Y.
78	US 2970226 A	19610131	22	Electronic timing device [TEXT AVAILABLE IN USOCR DATABASE]	SKELTON CHARLES W et al.
79	JP 03128522 A	19910531	18	DELAY CIRCUIT	ISHIHARA, TSUTOMU et al.
80	JP 60083416 A	19850511	5	DELAY CIRCUIT	KOYAMA, TAKAHIRO et al.
81	JP 54048147 A	19790416	6	DELAY PULSE GENERATOR CIRCUIT	NISHIMURA, TAKUMI
82	JP 52031640 A	19770310	3	PHSE DELAY CIRCUIT	YAMADA, KOICHI et al.
83	DE 4037048 A1	19920521	4	Delaying arbitrary sync. and async. rectangular signals - converting input signal into two mutually symmetrical intermediate signals and applying to RC low-pass filters and comparator	TUENGLER, VOLKER DR et al.

	Document ID	Issue Date	Pages	Title	Inventor
1	US 20070098128 A1	20070503	17	Test apparatus, clock generator and electronic device	Ishida; Masahiro et al.
2	US 20070075759 A1	20070405	12	Method and apparatus for delay line control using receive data	Metz; Peter C. et al.
3	US 20070075756 A1	20070405	10	Method and apparatus for trimming a phase detector in a delay-locked-loop	Metz; Peter C.
4	US 20070052463 A1	20070308	11	Method and apparatus for sigma-delta delay control in a Delay-Locked-Loop	Abel; Christopher J. et al.
5	US 20060214742 A1	20060928	26	Phase controlled oscillator circuit with input signal coupler	Dally; William J. et al.
6	US 20060139076 A1	20060629	14	Z-state circuit for delay-locked loops	Park; Sangbeom
7	US 20060132208 A1	20060622	21	Controllable idle time current mirror circuit for switching regulators, phase-locked loops, and delay-locked loops	Park; Sangbeom
8	US 20060125534 A1	20060615	22	Zero idle time Z-state circuit for phase-locked loops, delay-locked loops, and switching regulators	Park; Sangbeom
9	US 20050271131 A1	20051208	14	System and method for generating a jittered test signal	Hafed, Mohamed M. et al.
10	US 20050231291 A1	20051020	26	Phase controlled oscillator circuit with input signal coupler	Dally, William J. et al.
11	US 20050052252 A1	20050310	24	Synchronizing unit for redundant system clocks	Galibois, Joseph F.
12	US 20040012453 A1	20040122	25	Phase controlled oscillator	Dally, William J. et al.
13	US 20030177409 A1	20030918	31	Self-timed pipeline for tunable delays	Greenstreet, Mark R.

	Document ID	Issue Date	Pages	Title	Inventor
14	US 20020113660 A1	20020822	26	Phase controlled oscillator	Dally, William J. et al.
15	US 20020000791 A1	20020103	14	Vehicle alternator	Taniguchi, Makoto et al.
16	US 7215209 B2	20070508	20	Controllable idle time current mirror circuit for switching regulators, phase-locked loops, and delay-locked loops	Park; Sangbeom
17	US 7132869 B2	20061107	21	Zero idle time Z-state circuit for phase-locked loops, delay-locked loops, and switching regulators	Park; Sangbeom
18	US 7078979 B2	20060718	27	Phase controlled oscillator circuit with input signal coupler	Dally; William J. et al.
19	US 7073086 B2	20060704	28	System for controlling a tunable delay by transferring a signal from a first plurality of points along a first propagating circuit to a second plurality of points along a second propagating circuit	Greenstreet; Mark R.
20	US 6861916 B2	20050301	27	Phase controlled oscillator circuit with input signal coupler	Dally; William J. et al.
21	US 6617936 B2	20030909	26	Phase controlled oscillator	Dally; William J. et al.
22	US 6456048 B2	20020924	14	Vehicle alternator with anti-hunting feature and vehicle alternator control system	Taniguchi; Makoto et al.
23	US 5238380 A	19930824	13	Apparatus for precision volumetric control of a moldable material	Wenskus, Jr.; James J. et al.
24	US 5063008 A	19911105	12	Method for precision volumetric control of a moldable material in an injection molding process	Wenskus, Jr.; James J. et al.
25	US 4608723 A	19860902	10	Apparatus for lasting footwear	Giebel; Gerhard
26	US 4573900 A	19860304	17	Evacuation system for injection molding machines	Smith; Lyle
27	US 4546673 A	19851015	15	Control for vehicle provided with continuously variable speed system power transmission	Shigematsu; Takashi et al.
28	US 3720950 A	19730313	25	TIME-DOMAIN CORRELATOR FOR SPATIAL FILTERING IN A PULSED ENERGY SYSTEM	Vehrs, Jr.; Charles L.

	Document ID	Issue Date	Pages	Title	Inventor
29	US 20060267660 A	20061130	12	Receiver for performing clock and data recovery processing, has voltage-controlled delay loop that uses off-line interpolator to generate next clock signal to be injected into one of delay units	ABEL, C J et al.
30	US 20060114039 A	20060601	7	Clock signal generating method for use in voltage controlled delay loop, involves injecting reference clock into one delay line, providing output of line as clock signal, and shifting injection point of phase locked loop frequency	FREYMAN, R L et al.
31	DE 3925251 A	19900301	4	Diesel engine with temp.-dependent fuel injection - uses temp. sensor to delay injection when exhaust catalyst reaches activation temp.	MULLER, E
32	SU 1339396 A	19870923	3	Fluidic-jet type drops generator e.g. for computer print=out - has additional piezoelectric element and delay line for raising operating speed	RYBALKO, A G

	Type	Hits	Search Text
1	BRS	1276	375/224.ccls.
2	BRS	314	375/225.ccls.
3	BRS	253	375/226.ccls.
4	BRS	291	375/227.ccls.
5	BRS	2025	375/371.ccls.
6	BRS	681	375/373.ccls.
7	BRS	445	375/375.ccls.
8	BRS	2613	375/376.ccls.
9	BRS	858986	(jitter adj inject$3 or input$3 or insert$3) same (frequency multipl$4)
10	BRS	483	S1 and S9
11	BRS	530	S6 and S9
12	BRS	2	S16 and (inject$3 adj jitter)
13	BRS	1	S10 and S11
14	BRS	1012	S10 S11
15	BRS	998	S13 and (first frequency) and (second frequency)
16	BRS	896	S14 and reference

	DBs	Time Stamp	Comments	Error Definition	Errors	Ref #
1	US-PGPUB; USPAT; EPO; JPO; DERWENT	2007/07/26 08:59				S1
2	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:35				S2
3	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:35				S3
4	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:38				S4
5	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:38				S5
6	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:38				S6
7	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:39				S7
8	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:41				S8
9	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:43				S9
10	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:43				S10
11	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:03				S11
12	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:12				S18
13	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 11:44				S12
14	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:04				S13
15	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:05				S14
16	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:05				S15

	Type	Hits	Search Text
17	BRS	117	S16 and PLL
18	BRS	241	S14 and (reference adj signal)
19	BRS	74915	(jitter$3 clock) same (reference clock) same multipl$3
20	BRS	0	(jitter$3 adj1 clock) same (reference adj 1clock) same multipl$3
21	BRS	9	(jitter$3 adj1 clock) same (reference adj1 clock) same multipl$3
22	BRS	4887	324/765.ccls.
23	BRS	2599	S22 and (generat$3 jitter)
24	BRS	4	S22 and (generat$3 jitter) same (inject$2) same reference
25	BRS	1	S22 and (inject adj1 jitter)
26	BRS	1	S22 and (inject near3 jitter)
27	BRS	143	S22 and (inject or assert or input same jitter)
28	BRS	763	S22 and (inject or assert or input same jitter or noise or purtabation)
29	BRS	4912	S29 S30 S31 S32 S33 S34 S35
30	BRS	1279	375/224.ccls.
31	BRS	316	375/225.ccls.
32	BRS	256	375/226.ccls.

	DBs	Time Stamp	Comments	Error Definition	Errors	Ref #
17	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:06				S17
18	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/11/25 12:17				S16
19	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 15:54				S19
20	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 11:34				S20
21	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 11:34				S21
22	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 16:04				S22
23	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 15:54				S23
24	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 15:55				S24
25	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 16:05				S25
26	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 16:05				S26
27	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 17:28				S27
28	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/04 17:34				S28
29	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/05 07:33				S36
30	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S29
31	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S30
32	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S31

	Type	Hits	Search Text
33	BRS	293	375/227.ccls.
34	BRS	2030	375/371.ccls.
35	BRS	682	375/373.ccls.
36	BRS	447	375/375.ccls.
37	BRS	335	S36 and (jitter inject$3) same (scale$2 or multipl$3)
38	BRS	915	S36 and (jitter inject$3) and (scale$2 or multipl$3)
39	BRS	53	S38 and (generat$3 adj jitter or jitter adj generat$3)
40	BRS	335	S38 and (generat$3 jitter)
41	BRS	1282	375/224.ccls.
42	BRS	865311	(jitter adj inject$3 or input$3 or insert$3) same (frequency multipl$4)
43	BRS	487	S42 and S43
44	BRS	438	S44 and (frequency multiplier)
45	BRS	9	S44 and (frequency adj multiplier)
46	BRS	1	"06665808"
47	BRS	427	S44 and (frequency scaler)
48	BRS	1	"05835501"

	DBs	Time Stamp	Comments	Error Definition	Errors	Ref #
33	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S32
34	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S33
35	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S34
36	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/05 07:33				S35
37	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/05 09:14				S38
38	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/05 07:34				S37
39	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/05 09:15				S41
40	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/05 09:14				S40
41	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/24 09:55				S42
42	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/24 09:55				S43
43	US-PGPUB; USPAT; EPO; JPO; DERWENT	2006/12/24 10:00				S44
44	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 10:19				S45
45	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 09:57				S46
46	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 10:07				S47
47	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 10:19				S49
48	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 10:07				S48

	Type	Hits	Search Text
49	BRS	1	S44 and (frequency adj scaler)
50	BRS	381	S44 and (frequency adj scal$3 or multipl$4)
51	BRS	83	S54 and (timing error or jitter generat$3)
52	BRS	32	(jitter same injector) and (static delay line) and (control$4)
53	BRS	104	327/287.ccls.
54	BRS	30	S52 and (timi$3 error)

	DBs	Time Stamp	Comments	Error Definition	Errors	Ref #
49	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 10:20				S50
50	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2006/12/24 10:20				S51
51	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 10:09				S55
52	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:12				S52
53	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 10:08				S54
54	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 10:06				S53

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
1	BRS	L1	466578	(inject$3 or introduc$3 adj2 jitter) and (static delay line) and (control$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:13			
2	BRS	L2	130276	(inject$3 or introduc$3 adj2 jitter) same (static delay line) and (control$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:14			
3	BRS	L3	129989	(inject$3 or introduc$3 adj2 jitter adj1 generat$3) same (static delay line) and (control$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:15			
4	BRS	L4	114066	(inject$3 or introduc$3 adj2 jitter adj1 generat$3) same (static adj1 delay line) and (control$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:16			

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Errors
5	BRS	L5	44715	(inject$3 or introduc$3 adj2 jitter adj1 generat$3) same (static adj1 delay line) same (control$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:16			
6	BRS	L6	44715	(inject$3 or introduc$3 adj jitter adj1 generat$3) same (static adj1 delay line) same (control$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:16			
7	BRS	L7	32	(inject$3 or introduc$3 adj jitter adj generat$3) same (static adj1 delay line) same (control$4 adj1 delay)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT	2007/07/26 17:17			